[which comprises fabricating] providing a ring [counter] oscillator system clock having a plurality of transistors within the integrated circuit, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor; [and the microprocessor each having a plurality of transistors having operating characteristics which vary in the same way with variations in their fabrication,] and

using the ring [counter] oscillator system clock for clocking the microprocessor, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

66(Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, [and]

clocking the input/output interface with a second clock independent of the ring [counter] oscillator system clock, and

buffering information within said input/output interface received from said microprocessor integrated circuit.

Please add the following new claims 71-79:

71. The microprocessor system of claim 20 further including system memory coupled to said input/output interface, said system memory being synchronized to said second clock and operating synchronously with respect to said ring oscillator variable speed system clock.

72. The method of claim 65 further including the steps of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock.

73. A microprocessor system comprising:

a central processing unit disposed upon a substrate, said central processing unit operating at a processing frequency and including a first plurality of transistors;

an oscillator disposed upon said substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of transistors designed such that operating characteristics of said first plurality and said second plurality of transistors vary in the same way as a function of parameter variation in one or more operational parameters associated with said substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.//

74. The microprocessor system of claim 73 wherein said one or more parameters are included within the set consisting of: operating temperature of said substrate, operating voltage of said substrate, and fabrication process of said substrate.

75. The microprocessor system of claim 73 further comprising:

an input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, address and data with said central processing unit;

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

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~~76.~~ The microprocessor system of claim ~~75~~ wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

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~~77.~~ The microprocessor system of claim ~~73~~ wherein said oscillator comprises a ring oscillator.

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78. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon a substrate, said central processing unit including a first plurality of transistors and being operative at a processing frequency;

clocking said central processing unit at a clock rate using an oscillator disposed upon said substrate, said oscillator being provided so as to include a second plurality of transistors with said central processing unit being clocked by said oscillator at a variable frequency dependent upon variation in one or more operational parameters associated with said substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more operational parameters associated with said substrate.

79. The method of claim 78 further comprising the steps of:

connecting an input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, address and data between said input/output interface and said central processing unit;

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.